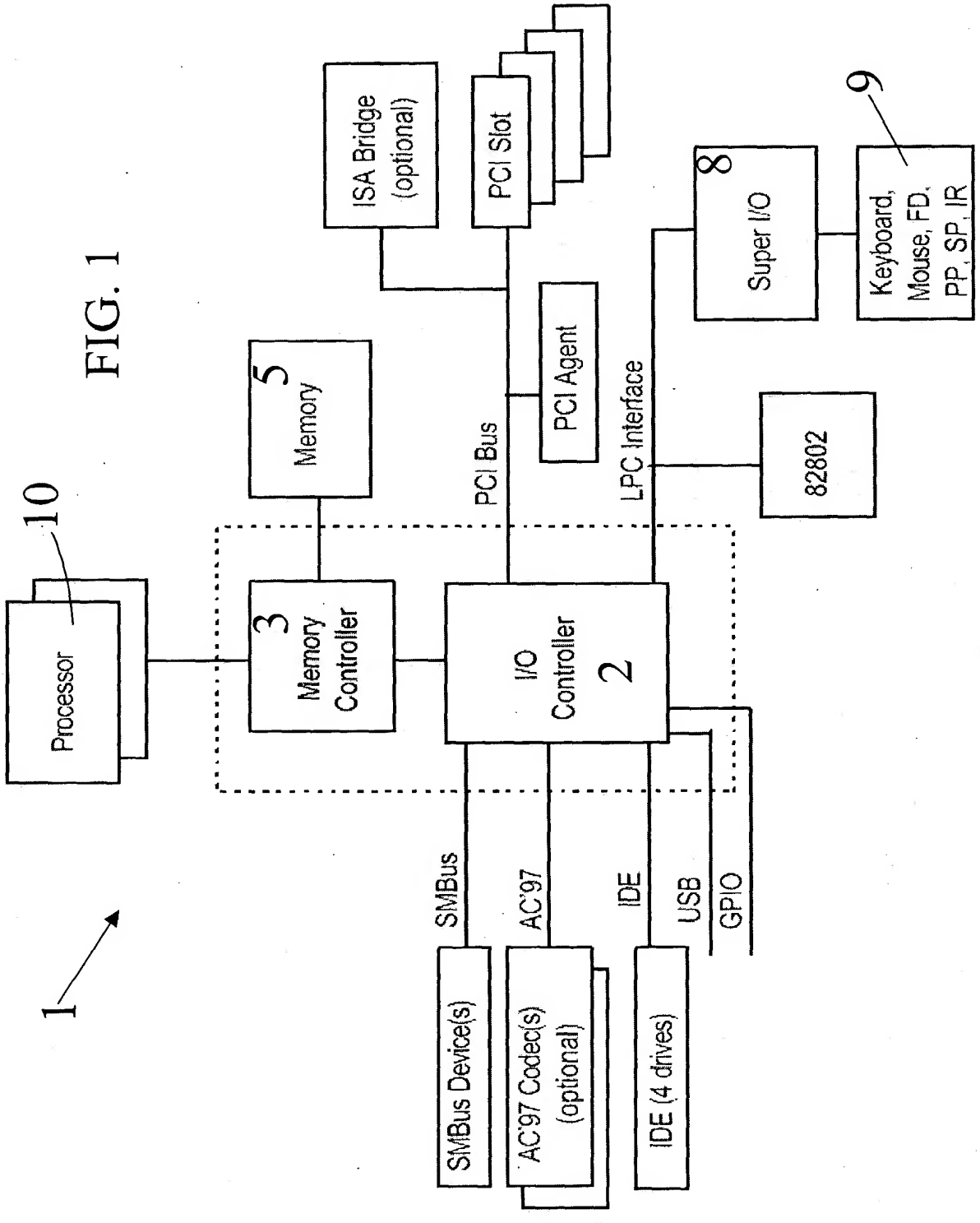
FIG. 1


1
Processor
10
3
Memory Controller
5
Memory
I/O Controller
2
PCI Bus
PCI Agent
ISA Bridge (optional)
PCI Slot
LPC Interface
82802
Super I/O
8
Keyboard, Mouse, FD, PP, SP, IR
9
SMBus
AC'97
IDE
USB
GPIO
SMBus Device(s)
AC'97 Codec(s) (optional)
IDE (4 drives)

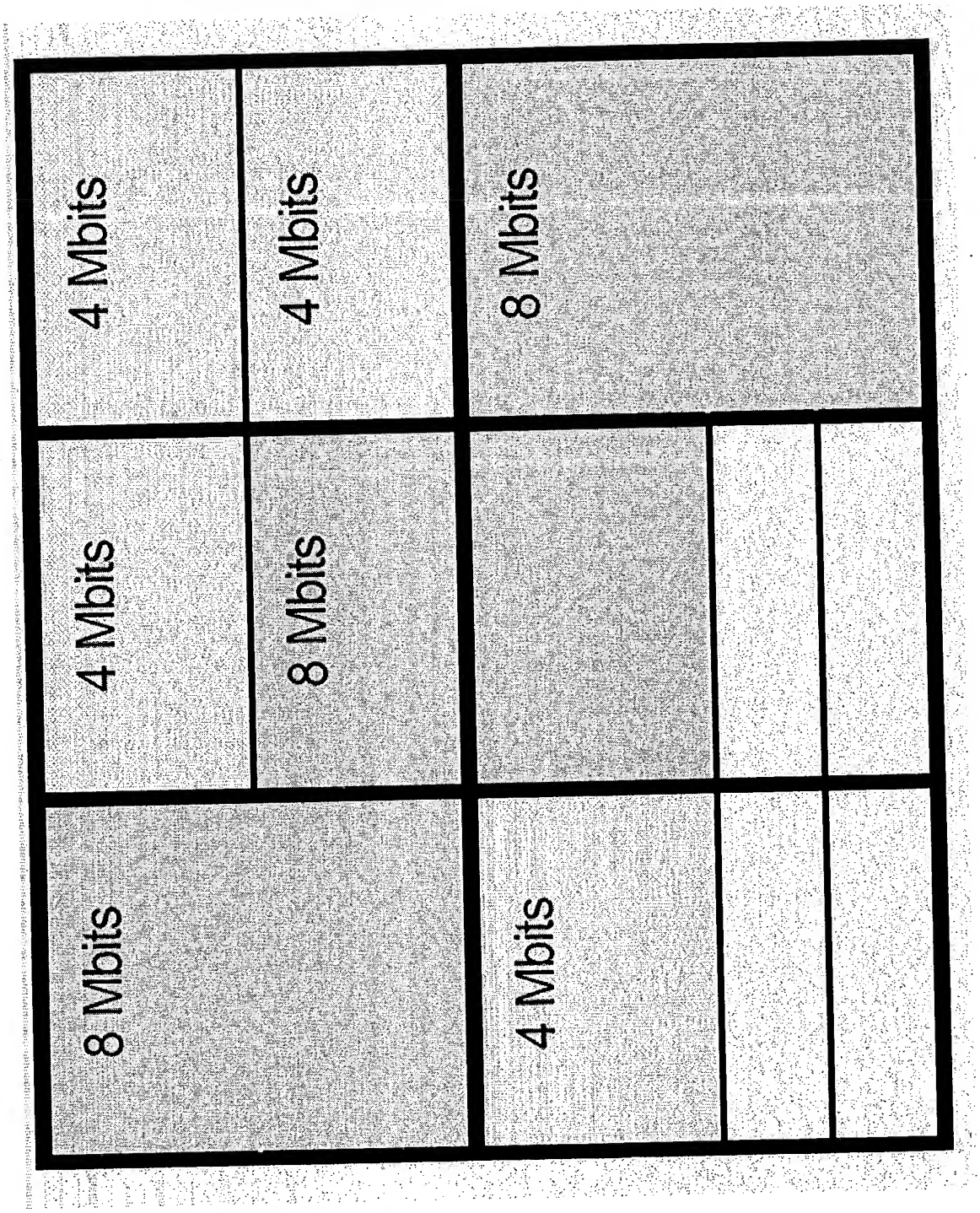


FIG. 2

FIG. 3

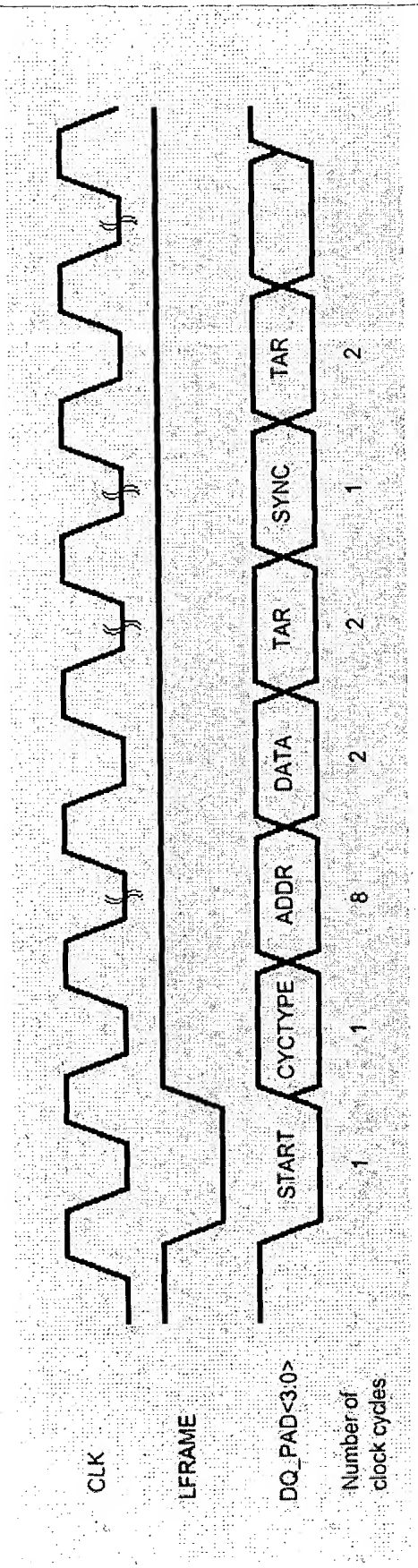
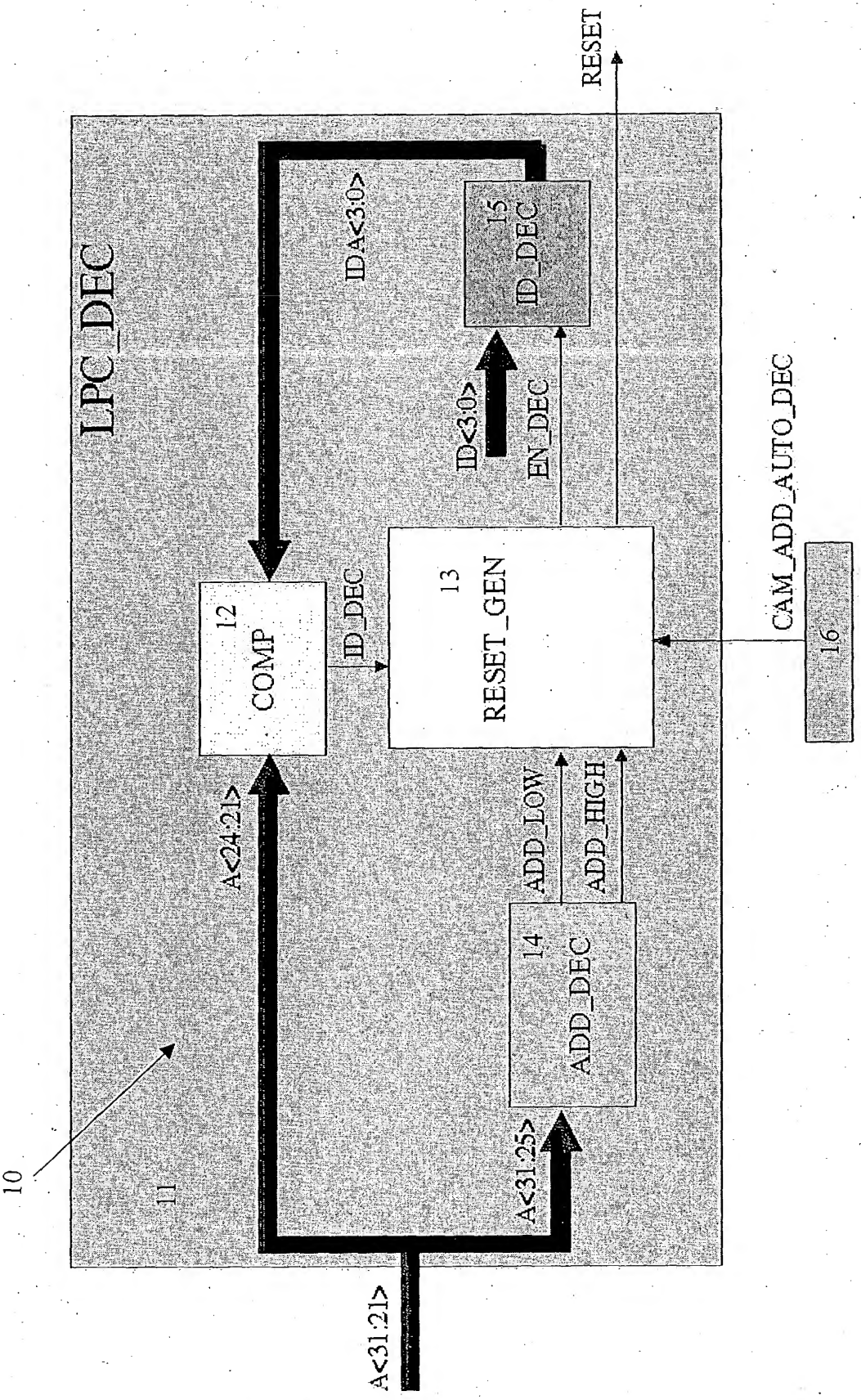

CLK
LFRAME
DQ_PAD<3:0>
START
CYCTYPE
ADDR
DATA
TAR
SYNC
TAR
Number of clock cycles
1
1
8
2
2
1
2

FIG. 4


RESET
LPC_DEC
ID.A<3:0>
15
ID_DEC
ID<3:0>
EN_DEC
12
COMP
ID_DEC
13
RESET_GEN
CAM_ADD_AUTO_DEC
16
A<24:21>
ADD_LOW
ADD_HIGH
14
ADD_DEC
A<31:25>
10
11
A<31:21>

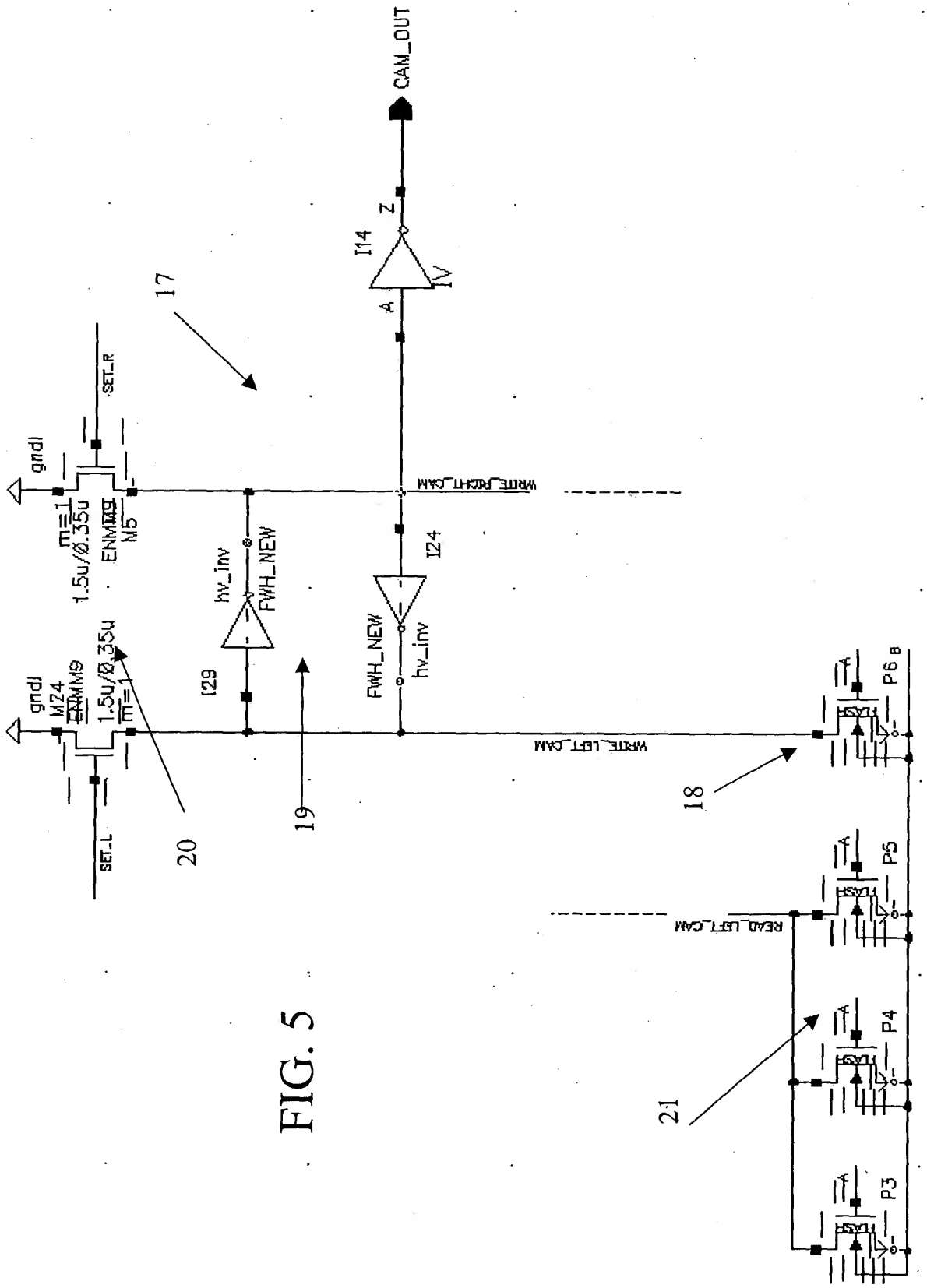

CAM_OUT
I14
Z
A
17
SET_R
gndl
m=1
1.5u/0.35u
M5
WRITE_RIGHT_CAM
I24
hv_inv
FWH_NEW
I29
M24
1.5u/0.35u
m=1
SET_L
20
19
18
WRITE_LEFT_CAM
P6
P5
READ_LEFT_CAM
P4
21
P3

FIG. 5

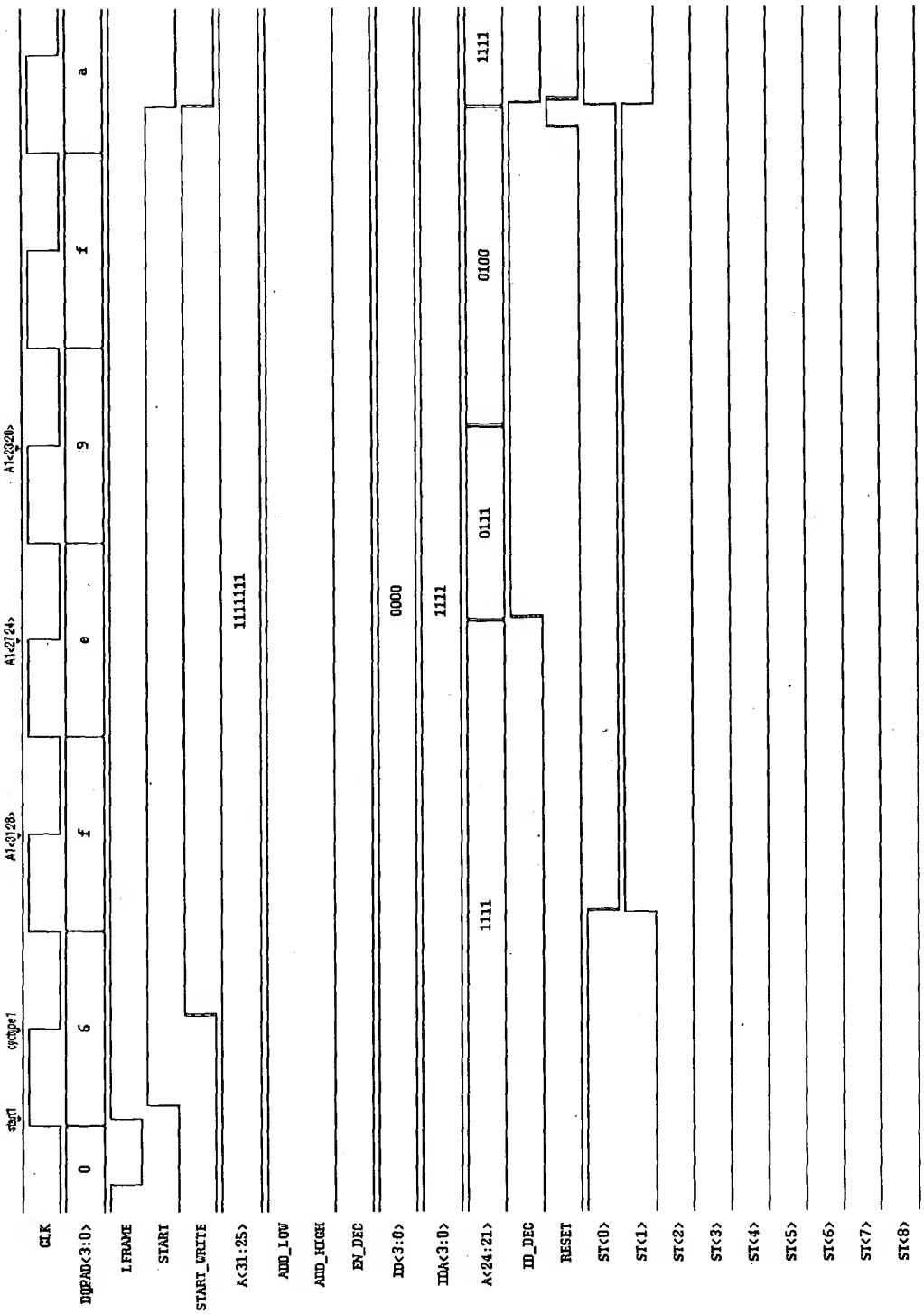

start
cycle1
A1<0128>
A1<2724>
A1<2320>
CLK
DQPAD<3:0>
0
6
f
e
9
f
a
LFRAME
START
START_WRITE
A<31:25>
1111111
ADD_LOW
ADD_HIGH
EN_DEC
ID<3:0>
0000
IDA<3:0>
1111
A<24:21>
1111
0111
0100
1111
ID_DEC
RESET
ST<0>
ST<1>
ST<2>
ST<3>
ST<4>
ST<5>
ST<6>
ST<7>
ST<8>

FIG. 6

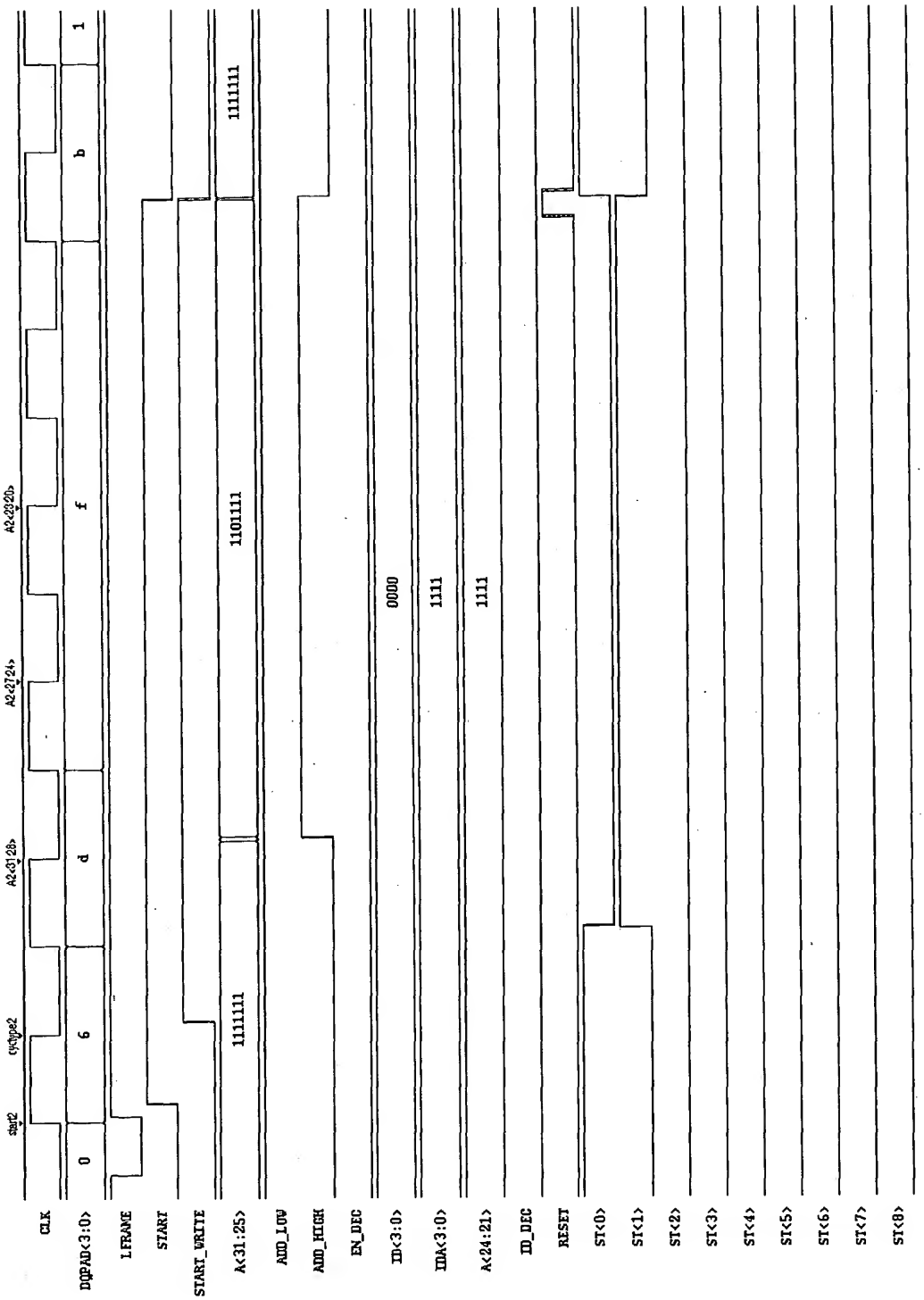

start2
cyctype2
A2<31:28>
A2<27:24>
A2<23:20>
CLK
DQPAD<3:0>
LFRAME
START
START_WRITE
A<31:25>
ADD_LOW
ADD_HIGH
EN_DEC
ID<3:0>
IDA<3:0>
A<24:21>
ID_DEC
RESET
ST<0>
ST<1>
ST<2>
ST<3>
ST<4>
ST<5>
ST<6>
ST<7>
ST<8>
0
6
d
f
b
1
1111111
1101111
0000
1111
1111

FIG. 7

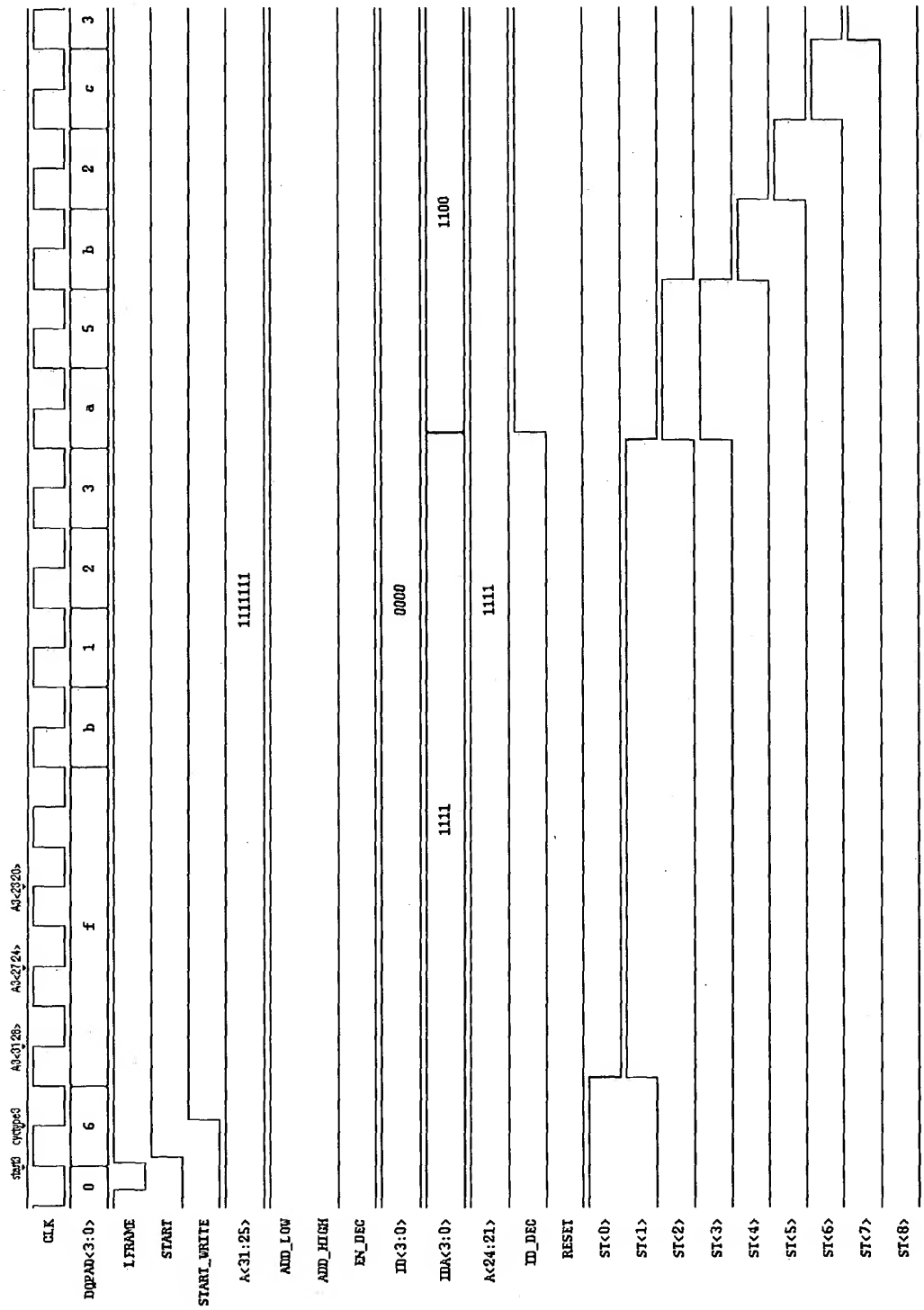

start0
cyctype3
A3<31:28>
A3<27:24>
A3<23:20>
CLK
DQPAD<3:0>
LFRAME
START
START_WRITE
A<31:25>
ADD_LOW
ADD_HIGH
EN_DEC
ID<3:0>
IDA<3:0>
A<24:21>
ID_DEC
RESET
ST<0>
ST<1>
ST<2>
ST<3>
ST<4>
ST<5>
ST<6>
ST<7>
ST<8>
0
6
f
b
1
2
3
a
5
b
2
c
3
1111111
0000
1111
1100
1111

FIG. 8

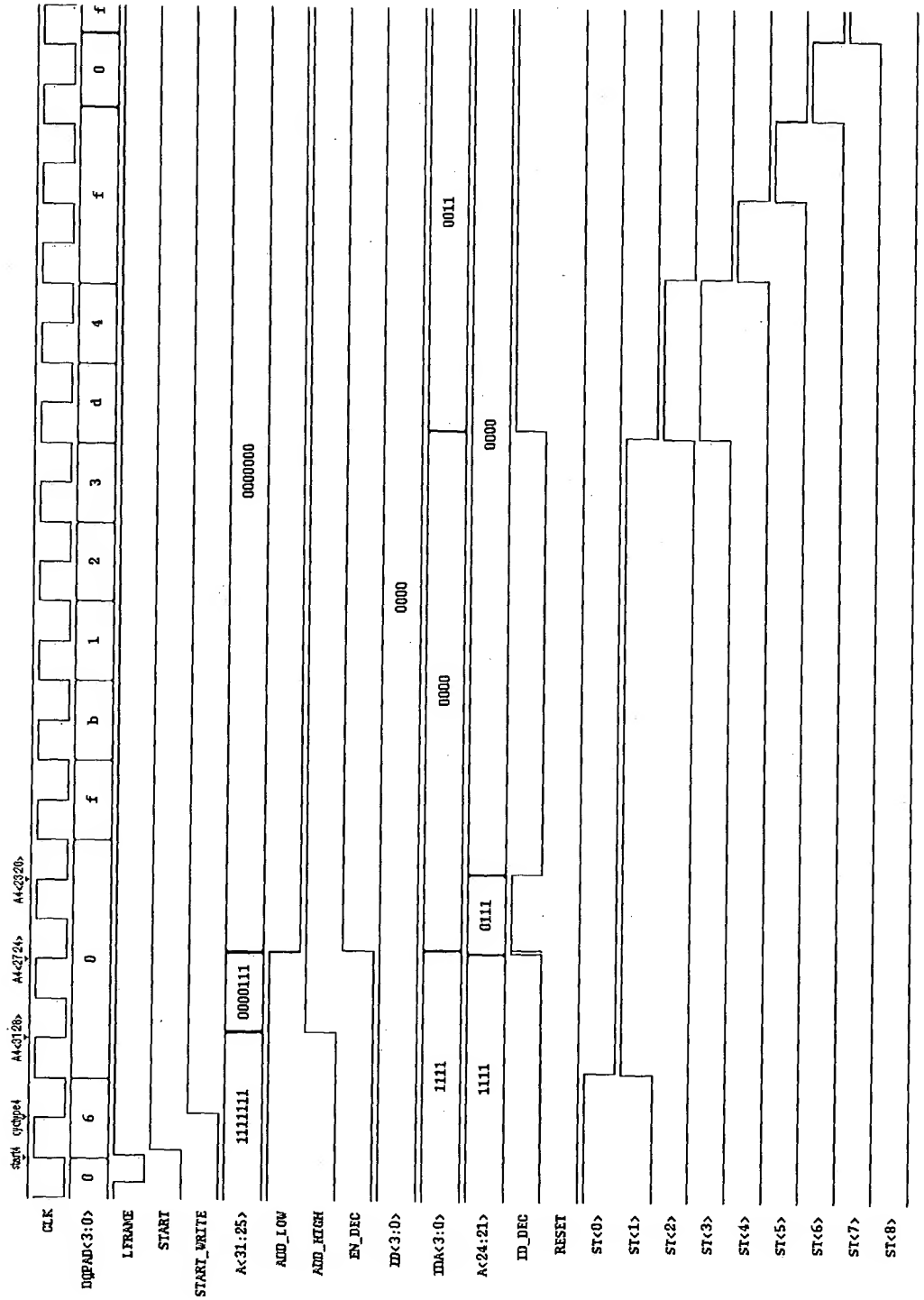

start
cycType
A<31:28>
A<27:24>
A<23:20>
CLK
LPCPAD<3:0>
LFRAME
START
START_WRITE
A<31:25>
ADD_LOW
ADD_HIGH
EN_DEC
ID<3:0>
IDA<3:0>
A<24:21>
ID_DEC
RESET
ST<0>
ST<1>
ST<2>
ST<3>
ST<4>
ST<5>
ST<6>
ST<7>
ST<8>
0
6
f
b
1
2
3
d
4
f
0
1111111
0000111
0000000
1111
1111
0000
0000
0011
0111
0000

FIG. 9